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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,752	01/02/2004	Wein-Town Sun	250122-1140	1840
24504	7590	06/01/2005		
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			EXAMINER FENTY, JESSE A	
			ART UNIT 2815	PAPER NUMBER

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/750,752

Applicant(s)

SUN, WEIN-TOWN

Examiner

Jesse A. Fenty

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 March 2005.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 7-21 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 8-20 is/are allowed.  
6) ☒ Claim(s) 1-5, 7 and 21 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 1-5 and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- a. In re claim 1, the specification does not explain what is meant by the term, “on different planes.”

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 7 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Katoh et al. (U.S. Patent No. 5,963,785).

In re claims 1, as best understood and 8, Katoh (esp. Fig. 3) discloses a semiconductor system and method of manufacturing the same, comprising:

a plurality of isolation substrates (9, 11), each isolation substrate having a circuit deposition region and a substrate-combining region;

a plurality of circuits (3, 7) formed on the circuit deposition regions;

a plurality of substrate-connecting elements (13, 17) formed to connect the substrate-combining regions; and

a plurality of electrical connecting elements (21, 23) formed to electrically connect the circuits formed on the different circuit deposition regions, wherein the circuit deposition region contact the substrate-combining region on different planes<sup>1</sup>

In re claims 2 and 4, Katoh discloses the device of claim 1. The limitations, “formed by heat fusing or laser” and “formed by laser fusing” refer to the processes for making this product. Applicant is reminded that, a Aproduct by process $\equiv$  claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a Aproduct by process $\equiv$  claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in Aproduct

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<sup>1</sup> In the Non-Final Office Action mailed 12/16/04, Examiner misinterpreted this limitation. Upon closer reading of the Specification, this limitation is interpreted to mean that the circuit deposition region and the substrate-combining region are simply two sides to the same block, as illustrated in Applicant's Figure 4. This limitation is anticipated by Fig. 3 of Katoh which also disclose a block region with horizontal and vertical sides, thus having regions that contact on different planes.

by process≡ claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

In re claim 7, Katoh discloses the device of claim 1, wherein the materials of the isolation substrates are glass (column 10, lines 65-67).

In re claim 21, Katoh discloses a method of manufacturing a semiconductor device, comprising the steps of:

providing a first isolation substrate (9) including a first circuit deposition region and a first substrate-combining region, and a second isolation substrate (11) including a second circuit deposition region and a second substrate-combining region;

forming a first circuit and a second circuit respectively on the first circuit deposition region and the second circuit deposition region, wherein the first circuit and the second circuit are packaged by different methods<sup>2</sup>;

forming a plurality of substrate-connecting elements (13, 15, 17, 19) for connecting the first substrate-combining region to the second substrate-combining region; and

forming a plurality of electrical connecting elements (21, 23) to electrically connect the first circuit and the second circuit.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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<sup>2</sup> That the first circuit and second circuit are formed by different methods is inherent in this device structure from the fact that the circuits contain different semiconductor elements. Forming a first circuit containing one set of elements will comprise different steps than forming a second circuit that contains a second set of different elements.

Art Unit: 2815

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim is rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh as applied to claim 1 above, and further in view of Liao et al. (U.S. Patent No. 6,689,636 B2).

In re claim 3, Katoh discloses the device claims 1, but does not expressly disclose the connecting elements being gold wires. Liao (esp. Fig. 8B) discloses the use of gold wires (30) in semiconductor packaging technology. It would have been obvious for one skilled in the art at the time of the invention to connect the substrates of Katoh with gold bond wires as disclosed by Liao for the purpose, for example, of providing enhanced electrical connections between the two surfaces (Liao; column 5, lines 34-37).

*Allowable Subject Matter*

5. Claim 8-20 are allowed.

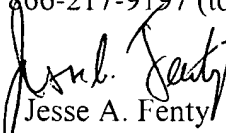
a. The following is a statement of reasons for the indication of allowable subject matter: In re claims 8 and 15, the method of manufacture including at least forming a plurality of substrate-connecting elements, wherein the first substrate substrate-combining region contacts the second substrate-combining region is neither anticipated nor obvious over the prior art of record.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Jesse A. Fenty  
Examiner  
Art Unit 2815